Refine Search

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Your result set for the last L# is incomplete.

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Search Results -

Terms	Documents
L8 same test$	17

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L12

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, February 28, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L12	L8 same test$	17	L12
L11	L10 same l5	4	L11
L10	test adj1 circuit	24862	L10
L9	L8 same l7	16	L9
L8	L5 same l6	65	L8
L7	enable adj1 signal	58926	L7
L6	reset adj1 signal	59034	L6
L5	L4 same input same output	346	L5
L4	L3 same signal same enable	447	L4
L3	L2 same control same circuit	1513	L3
L2	L1 same scan	4058	L2

L1	reset same (flip-flop or latch)	83936	L1

END OF SEARCH HISTORY

L9: Entry 2 of 16 File: USPT Oct 26, 1999

DOCUMENT-IDENTIFIER: US 5973529 A
TITLE: Pulse-to-static conversion latch with a self-timed control circuit

Detailed Description Text (21):
FIG. 15 is a schematic diagram of a preferred embodiment of the local buffer block 130 of FIG. 10, which buffers the LSSD data and controls, and the SRCMOS test-mode signals. This block basically consists of two sections, the upper portion of FIG. 15, which conditions the Scan.sub.-- Enable and RESET signals, and the lower portion, which buffers and distributes the scan-in data, the scan clocks, and the static-evaluate signals. The function of the Scan.sub.-- Enable signal is to prevent self-resetting of the latch-nodes during LSSD scanning. The purpose of the Scan.sub.-- Enable buffering circuits, shown in the upper portion of FIG. 15, are to insure that the Scan.sub.-- Enable signal utilized in the local clock and reset generation block 110 is synchronized to the global clock, CLKG. Such synchronization is desired so that single normal-operation cycles can be inserted among multiple scan cycles during LSSD testing. The scan enable path consists of an inverter, two transmission gates, two latches and one NMOS device. The scan enable signal is received by the input inverter/buffer 61. The output of buffer 61 is connected to the input of the first transmission gate TG10. The output of TG10 is connected to node A89. The gate of pMOS device Q91 is connected to node B2 and the gate of nMOS device Q92 is connected to node B3. Nodes B2 and B3 are located in the write-enable generator sub-block 120 within the MS1 circuit. The input of master latch FF19 is connected to node A89. The input of second transmission gate TG20 is connected to the node A90. The output of TG20 is connected to node A92. The gate of pMOS device Q93 is connected to node S43 and the gate of nMOS device Q94 is connected to the complement of node S43, node S44. There is also a scan-inhibit nMOS device QR70 connected to node A92. Activating the RESET signal (active-high) will turn on the nMOS device QR70, thereby pulling-down node A92, which inhibits scan operation.

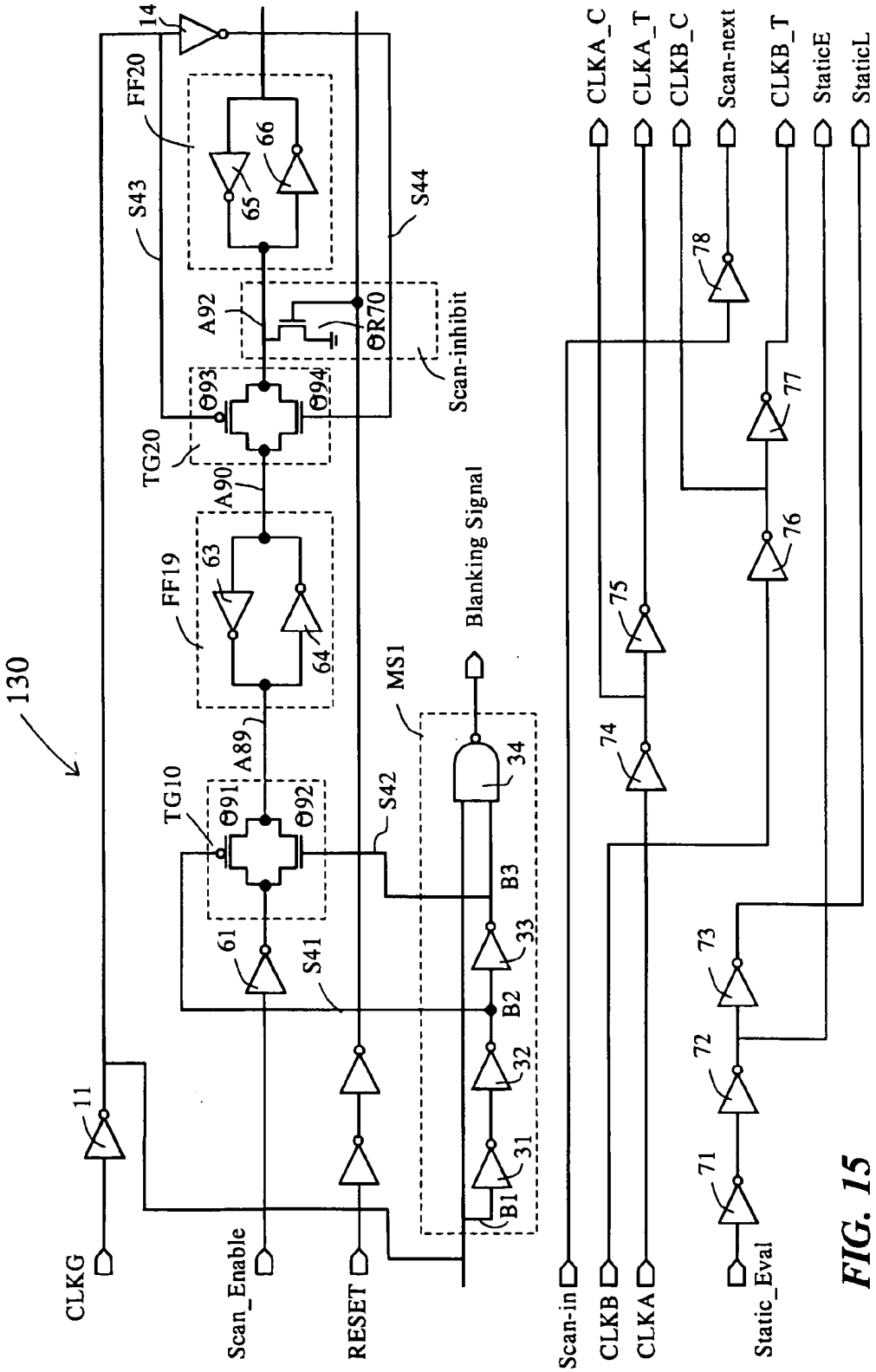
130
CLKG
Scan_Enable
RESET
Scan-in
CLKB
CLKA
Static_Eval
11
14
FF20
FF19
TG20
TG10
MS1
S41
S42
S43
S44
A89
A90
A92
Θ91
Θ92
Θ93
Θ94
ΘR70
61
63
64
65
66
31
32
33
34
71
72
73
74
75
76
77
78
B1
B2
B3
Blanking Signal
Scan-inhibit
CLKA_C
CLKA_T
CLKB_C
Scan-next
CLKB_T
StaticE
StaticL

FIG. 15

L9: Entry 3 of 16 File: USPT Aug 31, 1999

DOCUMENT-IDENTIFIER: US 5946247 A
** See image for Certificate of Correction **
TITLE: Semiconductor memory testing device

Detailed Description Text (10):
The operations of the scan register 231 having the aforementioned structure are now described. FIG. 2 is a timing chart showing an operation of incorporating data at the data input terminal D when the scan register 231 is employed as an output flip-flop of the semiconductor integrated circuit device (RAM) in a normal operation. As shown in FIG. 2, the clock signal (T) is transmitted to the timing signal input terminal T1 of the flip-flop circuit 234 as such through the OR circuit 235 when the shift inhibiting signal (SINH) is at a low level. When the comparison enable signal (CMPEN) is at a low level, the output of the NAND circuit 243 of the comparison circuit 232 regularly goes high and no reset signal (low-level signal) is generated, as shown in FIG. 2. When the shift mode control signal (SM) is at a low level on the leading edge of the clock signal (T), the selector circuit 233 selects the signal input terminal "0", so that the data input signal (D) from the semiconductor integrated circuit device (RAM) is incorporated in the flip-flop circuit 234.

Detailed Description Text (11):
FIG. 3 is a timing chart showing a shift operation of the flip-flop circuit 234 in initialization (setting "1") before starting a test of the semiconductor integrated circuit device (RAM) or in reading of a test result upon completion of the RAM test. As shown in FIG. 3, the clock signal (T) is transmitted to the timing signal input terminal T1 of the flip-flop circuit 234 as such through the OR circuit 235 when the shift inhibiting signal (SINH) is at a low level. When the comparison enable signal (CMPEN) is at a low level, no reset signal (low-level signal) is generated from the comparison circuit 232. When the shift mode control signal (SM) is at a high level on the leading edge of the clock signal (T), the selector circuit 233 selects the signal input terminal "1" so that the serial input signal (SI) is incorporated in the flip-flop circuit 234 and outputted to the data output terminal O1 (serial output terminal). The data output terminal O1 is connected to the signal input terminal ("1") of the next-stage scan register (see FIG. 23), so that the data is transmitted as a serial input signal (SO.Q=SI) for a shift operation.

Detailed Description Text (22):
Operations of the scan register 251 having the aforementioned structure are now described. FIG. 7 is a timing chart showing an operation of incorporating data at the data input terminal D when the scan register 251 is employed as an output flip-flop of the semiconductor integrated circuit device (RAM) in a normal operation. As shown in FIG. 7, the comparison circuit 232 generates no reset signal when a comparison enable signal (CMPEN) is at a low level. If the shift mode control signal (SM) is at a low level on the leading edge of the clock signal (T), the selector circuit 252 selects the signal input terminal "0", so that the data input signal (D) from the semiconductor integrated circuit device (RAM) is incorporated in the flip-flop circuit 234. Since the data output of the RAM is connected to the data input terminal D, the scan register 251 can be employed as an output flip-flop for the RAM in a normal operation.

Detailed Description Text (23):
FIG. 8 is a timing chart showing a shift operation. When the comparison enable signal (CMPEN) is at a low level, the comparison circuit 232 generates no reset signal. When the shift mode control signal (SM) and the shift inhibiting signal (SINH) are at high and low levels ("1" and "0") respectively on the leading edge of the clock signal (T), the serial input signal (SI) is incorporated in the flip-flop circuit 234 through the second selector circuit 253 and the first selector circuit 252, and outputted to the serial output terminal O1. The serial output terminal O1 is connected to a signal input terminal on a serial input signal (SI) side of a next-stage scan register, whereby a shift operation is carried out. The shift operation is carried out in initialization (setting "1") before starting of a RAM test or reading of a test result upon completion of the RAM test.

Detailed Description Text (25):
FIG. 10 is a timing chart showing a comparing operation. When the shift mode control signal (SM) and the shift inhibiting signal (SINH) are at high levels ("1") respectively on the leading edge of the clock signal (T), the output data SO.Q of the flip-flop circuit 234 is incorporated in the flip-flop circuit 234 itself through the selector circuits 253 and 252. Thus, the data is held. If the data at the data input terminal D and that at an expected data terminal (EXP) are different from each other when the clock signal (T) and the comparison enable signal (CMPEN) are at low and high levels respectively, the reset signal is generated to reset the flip-flop circuit 234 to "0". Since the flip-flop circuit 234 is set at "1" by the initializing shift operation, presence of a failure is stored due to its change to "0". Data on presence/absence of failures held in the scan register 231 are read after completion of the RAM test by a shift operation.

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L9: Entry 9 of 16 File: JPAB Jul 2, 2004

DOCUMENT-IDENTIFIER: JP 2004184316 A
TITLE: SCANNING TEST CIRCUIT

Abstract Text (2):
SOLUTION: This scanning test circuit 10 is characterized by being equipped with a flip-flop 100 having a reset input terminal R for inputting a reset signal RST, for inputting scan data SI and data DI, and acquiring output data DO by switching the inputted scan data and data by a scan shift enable signal SCAN_SE, and an AND gate 101 which is a reset control means for controlling a reset signal by the scan shift enable signal. This constitution has such an effect that the the number of LSI pins can be reduced because test dedicated pins such as pins for scanning test mode input dedicated for a scanning test or for external reset input are not required to be installed separately.

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L9: Entry 9 of 16 File: JPAB Jul 2, 2004

PUB-NO: JP02004184316A
DOCUMENT-IDENTIFIER: JP 2004184316 A
TITLE: SCANNING TEST CIRCUIT

PUBN-DATE: July 2, 2004

INVENTOR-INFORMATION:

NAME	COUNTRY
NATSUME, KENICHI	

ASSIGNEE-INFORMATION:

NAME	COUNTRY
OKI ELECTRIC IND CO LTD	

APPL-NO: JP2002353702
APPL-DATE: December 5, 2002

INT-CL (IPC): G01 R 31/28; H01 L 21/822; H01 L 27/04

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a scanning test circuit capable of reducing the number of LSI pins, reducing test patterns, improving a failure detection rate, and reducing a scanning test related circuit scale.

SOLUTION: This scanning test circuit 10 is characterized by being equipped with a flip-flop 100 having a reset input terminal R for inputting a reset signal RST, for inputting scan data SI and data DI, and acquiring output data DO by switching the inputted scan data and data by a scan shift enable signal SCAN_SE, and an AND gate 101 which is a reset control means for controlling a reset signal by the scan shift enable signal. This constitution has such an effect that the the number of LSI pins can be reduced because test dedicated pins such as pins for scanning test mode input dedicated for a scanning test or for external reset input are not required to be installed separately.

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L11: Entry 1 of 4 File: USPT Apr 26, 2005

DOCUMENT-IDENTIFIER: US 6886124 B2
TITLE: Low hardware overhead scan based 3-weight weighted random BIST architectures

Brief Summary Text (75):
Another aspect of the claimed invention, is a parallel type test per scan built-in self test circuit comprising a circuit under test comprising inputs. A set of scan flip flops are connected to the inputs. Each of the scan flip flops have at least a synchronous reset (R) or a synchronous preset (S) pin. A LFSR is provided for loading random vectors that provide input to the set of scan flip-flops. A decoder provides decoder outputs, wherein the decoder outputs control the R and S pins in the scan flip-flops. The decoder comprises a functionality of a global generator. A counter provides inputs to the decoder that determine a state of the decoder outputs. An enable provides inputs for the decoder. The decoder provides overriding signals to inputs of the circuit by controlling the input to the R and S pins. The overriding signals override the random vectors based on inputs in a generator for test patterns for hard faults, said tests being generated by an automatic test pattern generator.

CLAIMS:

15. A parallel type test per scan built-in self test circuit comprising: a circuit under test comprising inputs; a set of scan flip flops that are connected to the inputs, each of said scan flip flops having at least a synchronous reset (R) or a synchronous preset (S) pin; a LFSR for loading random vectors that provide input to the set of scan flip-flops; a decoder providing decoder outputs, wherein said decoder outputs control the R and S pins in the scan flip-flops, said decoder comprising a functionality of a global generator; a counter providing inputs to the decoder that determine a state of the decoder outputs; and an enable input for the decoder, wherein the decoder provides overriding signals to by controlling the input to the R and S pins, said overriding signals overriding the random vectors based on tests in a generator for test patterns for hard faults, said tests being generated by an automatic test pattern generator.

L12: Entry 2 of 17 File: USPT Oct 26, 1999

DOCUMENT-IDENTIFIER: US 5973529 A
TITLE: Pulse-to-static conversion latch with a self-timed control circuit

Detailed Description Text (21):
FIG. 15 is a schematic diagram of a preferred embodiment of the local buffer block 130 of FIG. 10, which buffers the LSSD data and controls, and the SRCMOS test-mode signals. This block basically consists of two sections, the upper portion of FIG. 15, which conditions the Scan.sub.-- Enable and RESET signals, and the lower portion, which buffers and distributes the scan-in data, the scan clocks, and the static-evaluate signals. The function of the Scan.sub.-- Enable signal is to prevent self-resetting of the latch-nodes during LSSD scanning. The purpose of the Scan.sub.-- Enable buffering circuits, shown in the upper portion of FIG. 15, are to insure that the Scan.sub.-- Enable signal utilized in the local clock and reset generation block 110 is synchronized to the global clock, CLKG. Such synchronization is desired so that single normal-operation cycles can be inserted among multiple scan cycles during LSSD testing. The scan enable path consists of an inverter, two transmission gates, two latches and one NMOS device. The scan enable signal is received by the input inverter/buffer 61. The output of buffer 61 is connected to the input of the first transmission gate TG10. The output of TG10 is connected to node A89. The gate of pMOS device Q91 is connected to node B2 and the gate of nMOS device Q92 is connected to node B3. Nodes B2 and B3 are located in the write-enable generator sub-block 120 within the MS1 circuit. The input of master latch FF19 is connected to node A89. The input of second transmission gate TG20 is connected to the node A90. The output of TG20 is connected to node A92. The gate of pMOS device Q93 is connected to node S43 and the gate of nMOS device Q94 is connected to the complement of node S43, node S44. There is also a scan-inhibit nMOS device QR70 connected to node A92. Activating the RESET signal (active-high) will turn on the nMOS device QR70, thereby pulling-down node A92, which inhibits scan operation.

L12: Entry 4 of 17 File: USPT Jun 8, 1999

DOCUMENT-IDENTIFIER: US 5911039 A
TITLE: Integrated circuit device comprising a plurality of functional modules each performing predetermined function

Detailed Description Text (6):
In the scan path selecting circuit 5 shown in FIG. 2, the D latches 15 and 16 each having the reset function are connected in series and function as a shift register. That is, a signal held in the master latch 15 is outputted from the scan path enable terminal 21 and supplied to the output control signal line of the tri-state buffer 4 (FIG. 1). A selecting signal or test command signal SSI (FIG. 3) on the shift path 8 (FIG. 1) is inputted to the D latch 15 through a selecting data input terminal 17 and then the shift register comprising the D latches 15 and 16 performs a shift operation in response to non-overlapped two-phased clocks T1 and T2 (FIG. 3) applied through the shift clock terminals 18 and 19 from the control signal line 9 of FIG. 1. Then, the selecting signal SSO (FIG. 3) is outputted onto the shift path 8 through the selecting data output terminal 22. The data of the D latches 15 and 16 is fixed to an "L" (logical low) level in response to a reset signal inputted through the reset signal input terminal 20.

L12: Entry 5 of 17 File: USPT Sep 29, 1998

DOCUMENT-IDENTIFIER: US 5815512 A
TITLE: Semiconductor memory testing device

Detailed Description Text (11):
FIG. 3 is a timing chart showing a shift operation of the flip-flop circuit 234 in initialization (setting "1") before starting a test of the semiconductor integrated circuit device (RAM) or in reading of a test result upon completion of the RAM test. As shown in FIG. 3, the clock signal (T) is transmitted to the timing signal input terminal T1 of the flip-flop circuit 234 as such through the OR circuit 235 when the shift inhibiting signal (SINH) is at a low level. When the comparison enable signal (CMPEN) is at a low level, no reset signal (low-level signal) is generated from the comparison circuit 232. When the shift mode control signal (SM) is at a high level on the leading edge of the clock signal (T), the selector circuit 233 selects the signal input terminal "1" so that the serial input signal (SI) is incorporated in the flip-flop circuit 234 and outputted to the data output terminal 01 (serial output terminal). The data output terminal 01 is connected to the signal input terminal ("1") of the next-stage scan register (see FIG. 23), so that the data is transmitted as a serial input signal (SO.Q=SI) for a shift operation.

Detailed Description Text (23):
FIG. 8 is a timing chart showing a shift operation. When the comparison enable signal (CMPEN) is at a low level, the comparison circuit 232 generates no reset signal. When the shift mode control signal (SM) and the shift inhibiting signal (SINH) are at high and low levels ("1" and "0") respectively on the leading edge of the clock signal (T), the serial input signal (SI) is incorporated in the flip-flop circuit 234 through the second selector circuit 253 and the first selector circuit 252, and outputted to the serial output terminal O1. The serial output terminal O1 is connected to a signal input terminal on a serial input signal (SI) side of a next-stage scan register, whereby a shift operation is carried out. The shift operation is carried out in initialization (setting "1") before starting of a RAM test or reading of a test result upon completion of the RAM test.

Detailed Description Text (25):
FIG. 10 is a timing chart showing a comparing operation. When the shift mode control signal (SM) and the shift inhibiting signal (SINH) are at high levels ("1") respectively on the leading edge of the clock signal (T), the output data SO.Q of the flip-flop circuit 234 is incorporated in the flip-flop circuit 234 itself through the selector circuits 253 and 252. Thus, the data is held. If the data at the data input terminal D and that at an expected data terminal (EXP) are different from each other when the clock signal (T) and the comparison enable signal (CMPEN) are at low and high levels respectively, the reset signal is generated to reset the flip-flop circuit 234 to "0". Since the flip-flop circuit 234 is set at "1" by the initializing shift operation, presence of a failure is stored due to its change to "0". Data on presence/absence of failures held in the scan register 231 are read after completion of the RAM test by a shift operation.

US 20040153915A1

(19) United States

(12) Patent Application Publication (10) Pub. No.: US 2004/0153915 A1

McLaurin (43) Pub. Date: Aug. 5, 2004

(54) RESETTING LATCH CIRCUITS WITHIN A FUNCTIONAL CIRCUIT AND A TEST WRAPPER CIRCUIT

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(21) Appl. No.: 10/356,587

(22) Filed: Feb. 3, 2003

Publication Classification

(51) Int. Cl.[7] G01R 31/28

(52) U.S. Cl. 714/724

(57) ABSTRACT

Within an integrated circuit **2** a functional block of circuitry **6** has an associated test wrapper circuit **10**. The functional block of circuitry **6** includes functional latches **14** at least some of which may also serve as shared test latches **18** within the test wrapper circuitry **10**. Separate reset signals reset_wrp, reset_int are generated for the test latches and shared test latches **18** as distinct from the functional latches **14**. Thus, during testing, power consuming activity of the functional latches **14** can be suppressed if it is not desired to test the functional block of circuitry **6** itself. This is a particularly useful technique when a functional block of circuitry **6** is required to operate in an extest mode in which output signals from it are required to be driven so that other elements in the overall design may be tested and yet the internal action of the functional block of circuity **6** is not under test.